REMARKS/ARGUMENTS

Claims 1-35 are pending in the present application, with Claims 1-5, 7-9 and 11-16 standing rejected. Applicant acknowledges with appreciation the allowance of Claims 18-35, and the indication of allowable subject matter in Claims 6, 10 and 17. Reconsideration and allowance of the rejected claims is respectfully requested in view of the remarks presented below.

The Examiner rejected Claims 1-5, 7-9 and 11-16 under 35 U.S.C. § 103(a) as being unpatentable over Yamano (U.S. Patent No. 5,677,874). The Examiner relies on Yamano as the primary reference and acknowledges that certain limitations from each of the rejected claims are not disclosed therein. To cure the deficiencies in Yamano, the Examiner alleges that the missing limitations are "old and well-known in the art." These rejections are respectfully traversed.

Obviousness rejections based on an Examiner taking "official notice of facts not in the record" or relying on "common knowledge" are described in MPEP § 2144. According to the MPEP, such rejections are disfavored and are only appropriate in limited circumstances. Such rejections should be limited to the assertion of facts that are "capable of such instant and unquestionable demonstration as to defy dispute," and ordinarily there must be evidence to support an assertion of common knowledge. *See, e.g.*, MPEP § 2144.03. If an Applicant adequately traverses the Examiner's rejection, the Examiner must provide documentary evidence in the next Office Action if the rejection is to be maintained. *See* 37 CFR 1.104(c)(2). If the Examiner is relying on personal knowledge to support the finding of what is known in the art, the Examiner will be required to provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. *See* 37 CFR 1.104(d)(2).

Turning to Claims 1, 11, 12, 15 and 16, the Examiner admits that Yamano does not disclose the claimed "voltage control means," and argues that "such circuits are old and well-known in the art, as shown by several references included on the attached PTO-892 form." None of the cited references explicitly identifies a "voltage control means" and the Examiner does not identify the portions of any cited reference that discloses the alleged old and well-

known art. As a result, the scope of the subject matter that the Examiner alleges is "old and well-known in the art" is unclear, and the rejection is not "capable of such instant and unquestionable demonstration as to defy dispute" as required under MPEP 2144.

Moreover, there is no teaching, suggestion or motivation to combine the claimed "voltage control means" with Yamano. The Examiner argues that such circuitry would "allow accurate control of the pumping circuit" in Yamano. There is no disclosure or suggestion, however, that more "accurate control of the pumping circuitry" of Yamano would be desired. It is well settled that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP § 2143.01.

The cited prior art also fails to disclose or suggest other limitations of Claim 1 including "an output voltage control means connected to a voltage booster circuit adjacent to a final stage of said voltage booster circuits." As discussed above, Yamano fails to teach or disclose "an output voltage control means" and, further, there is no teaching or suggestion of the claimed connection between the voltage control means and the final stage of the voltage booster circuits.

The Examiner also admits that Yamano does not disclose "the capacitor and diode within the pump circuit 7" of Claim 1, but argues that "such elements are old and well-known in the art for forming a pump circuit." The Examiner states that the "motivation for using a capacitor and diode to make pump circuit 7 is simply to utilize the most well-known pump structure." This rejection is respectfully traversed. First, the Examiner does not clearly identify "the most well-known pump structure," nor is there any documentary proof to establish that the claimed structure is "the most well-known." Second, referring to Fig. 10 of Yamano, Yamano discloses a different pump circuit design that does not disclose or suggest the claimed elements, and thus teaches away from the suggestion that Yamano would be motivated to use the alleged "most well-known pump structure."

The Examiner also admits that Yamano does not disclose the formation of the various elements on a single semiconductor substrate as recited in Claim 1, but argues that "it is old and well-known in the art to put as much integrated circuits as possible into a single chip

...the motivation to form compact 'single unit' IC." In contrast to the Examiner's assertions, Applicant respectfully submits that it is not always possible, practical or desirable to form a single unit integrated circuit. There is no teaching or suggestion in Yamano, in view of the other cited prior art, of forming the claimed combination of elements on a single substrate.

Because Yamano, in view of the Examiner's assertions of what was "old and well-known in the art," does not teach or suggest every limitation of Claim 1, Claim 1 is allowable over the prior art.

Referring to Claim 2, the Examiner applies the same rejection as Claim 1, the "only difference in claim 2 being that the pump is upstream of the DC-DC converter, instead of downstream thereof." The Examiner argues that "it is old and well-known in the art that a pair of series-connected elements (i.e., cascaded input-to-output) ...can be connected in any order, without any unexpected change in circuit operation or result." Initially, Applicant respectfully notes that the Examiner's rejection is overcome because neither claim 1 nor claim 2 recite a "DC-DC converter," *per se*. Further, Claim 2 is allowable for the same reasons as Claim 1, discussed above. Moreover, Applicant respectfully submits that it is unclear what the Examiner means by "connected in any order, without any unexpected change in circuit operation or result." Yamano discloses and claims an arrangement for a DC-DC converter and pumping circuit, and does not suggest that such elements can be arranged in another order.

Regarding Claims 3-5, the Examiner argues that "the recited boost ratios and supply levels are deemed to be obvious design expedients to any person having ordinary skill in the art who will easily recognize that the pumping circuits of Yamano can be set to any desired values, as can the supply voltage Vcc." Applicant respectfully submits that there is no disclosure or suggestion that the "pumping circuits of Yamano can be set to 'any desired values.'" Claims 7 and 8 are similarly rejected based on Examiner assertions of what is known in the art. In any event, the rejections of dependent Claims 3-5, 7 and 8 are moot in view the arguments presented above regarding the allowability of independent Claim 1.

The Examiner rejected Claims 9 and 14 by asserting that "the recited inductor structure does not define over Yamano because it is also old and well-known in the art to

form inductors on IC chips in this manner." This rejection essentially provides a generic and conclusory statement that Claim 9 is "old and well known," and is not sufficient to establish a prima facie for obviousness. Further, as discussed herein, Claims 9 and 14 depend from allowable independent claims rendering this rejection moot. Regardless, there is no disclosure or suggestion in the prior art of a "parallel connection type inductance element consisting essentially of multilayered metal wiring layers and a dielectric film provided between the wiring layers, with said multilayered metal wiring layers being connected in parallel," as recited in Claim 9, nor "a parallel-connection type inductance element with multilayered metal wires being connected in parallel," as recited in Claim 14.

Regarding Claim 13, the Examiner argues that "the limitation of forming the inductor wiring at the same time as forming other wiring of the circuitry shown in Figs. 103 of Yamano also would have been obvious because simultaneous formation of metal wires on an IC is also old and well-known in the art of semiconductor manufacturing." This rejection is respectfully traversed, because the Examiner has failed to establish that each and every limitation of Claim 13 is disclosed or suggested by the prior art. For example, there is no suggestion or disclosure of "a voltage control unit," "a converter circuit" and "said inductance element of said converter circuit at least includes a metal wire to be formed at the same time during formation of either a signal wire of said internal element or a metal wire used for power supply wiring" as recited in Claim 13.

The Examiner objected to each of Claims 6, 10 and 17 as being dependent upon a rejected base claim, and indicated that each claim would be allowable if rewritten in independent form. Applicant respectfully submits that this objection has been traversed in view of the remarks, presented above, regarding the allowability of independent Claims 1 and 13. Rejected Claims 11, 12, 15 and 16 also depend from allowable independent claims and are similarly allowable.

Applicant respectfully submits that the application is now in condition for allowance. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

If necessary to effect a timely response, this paper should be considered as a petition for an Extension of Time sufficient to effect a timely response. Please charge any such fee or any deficiency in fees, or credit any overpayment of fees, to Deposit Account No. 05-1323 (Docket No.: 056203.55676US).

Respectfully submitted,

CROWELL & MORING LLP

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